Chapter 3

Digital Radio Systems

3.1 Introduction

Digital communication systems offer several outstanding advantages over traditional analogue systems: Ease of processing, ease of multiplexing, and noise immunity.

Traditional electronic communications systems that use conventional analogue techniques, such as amplitude modulation AM, frequency modulation FM, and phase modulation PM are generally being replaced with more modern digital communication systems.

Electronic communications is the transmission, reception, and processing of information using electronic circuits. Information is defined as knowledge or intelligence communicated or received. Information is propagated through a system in the form of symbols which can be:

- Analogue (continuous proportional), such as the human voice, video picture, or music.
- Digital (discrete), such as binary-coded numbers, graphic symbols, microprocessor operational codes, or data base information.

The information capacity of a communication system is the number of independent symbols that can be carried through the system in a given unit of time. In 1928 Hartley's law developed a useful relationship among bandwidth *B*, time *T*, and information capacity *C*:

$$C \alpha BxT \tag{3.1}$$

If either the bandwidth or the transmission time is changed, a directly proportional change in information capacity will occur. In 1948 Shannon published a limit for information capacity:

$$C = B\log_2\left(1+\frac{S}{N}\right) = 3.32\,B\log_{10}\left(1+\frac{S}{N}\right) \tag{3.2}$$

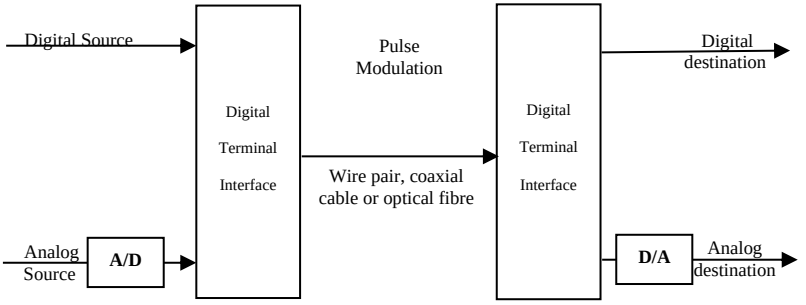
For a standard voice communication channel with a signal to noise power ratio of 1000 (i.e., 30 dB) and a bandwidth of 2.7 kHz, the Shannon limit for information capacity is then:

$$C = 2700\log_2(1+1000) = 26.9\ kbps$$

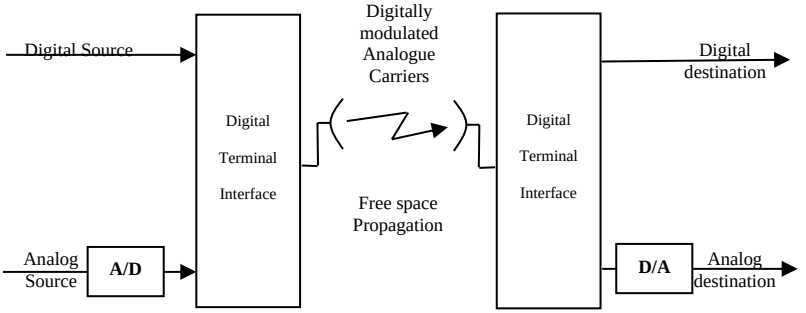
This limit is often misunderstood. The above example may be true, but it cannot be done with a binary system. To achieve an information transmission rate of 26.9 kbps through a 2.7 kHz channel, each symbol transmitted must contain more than one bit of information. Therefore, to achieve the Shannon limit, digital transmission systems that have more than two output conditions

(symbols) must be used. Several such systems are described in the following chapter. These systems include both analogue and digital modulation techniques and the transmission of both.

Digital communications covers a broad area of communications techniques including baseband transmission and radio transmission. Baseband transmission is the transmittal of pulses between two or more points in the baseband of the communication channel. Digital radio transmission is the transmittal of ***digitally modulated*** **analogue** ***carriers*** between two or more points in the passband (e.g. at the radio frequencies) of the communication channel. The difference between the baseband and digital radio communications is illustrated in Fig.3.1.



(a) Baseband Transmission



(b) Digital Radio Transmission

Fig.3.1: Digital Communication

The property that distinguishes a digital radio system from a conventional AM, FM, or PM radio system is that in a digital radio system the modulating and demodulated signals are digital pulses rather than analogue waveforms. However, digital radio uses analogue carriers just as conventional system do. Essentially, there are three basic digital radio modulation techniques: frequency shift keying FSK, phase shift keying, PSK, and ASK. Nevertheless, there are three techniques that are commonly used in digital radio systems. These are FSK, PSK, and quadrature amplitude modulation QAM.

3.2 Frequency Shift Keying FSK

Frequency shift keying is a simple, low performance form of digital modulation. Binary FSK is a constant envelope angle modulation similar to conventional FM except that the modulating signal is a binary pulse stream varies between two discrete voltage levels rather than a continuously changing analogue waveform. With a carrier amplitude V_c, frequency deviation ω_c, and frequency shift $\Delta\omega$, FSK voltage for binary digital modulating signal $f_m(t)$ is:

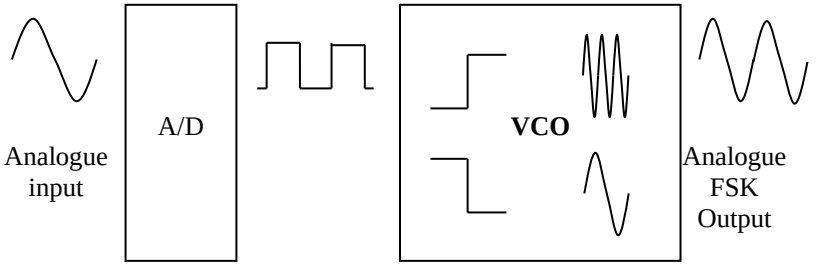
$$v(t) = V_c \cos\left[\left(\omega_c + \frac{f_m(t)\Delta\omega}{2}\right)t\right] \qquad (3.3)$$

So, the carrier amplitude remains constant, whereas its frequency ω_c shifts by $\pm\Delta\omega$. The carrier frequency shift rate equals the input bit rate (ω_c shifts between ω_c-Δω/2 and ω_c+Δω/2 at a rate equal to f_b.

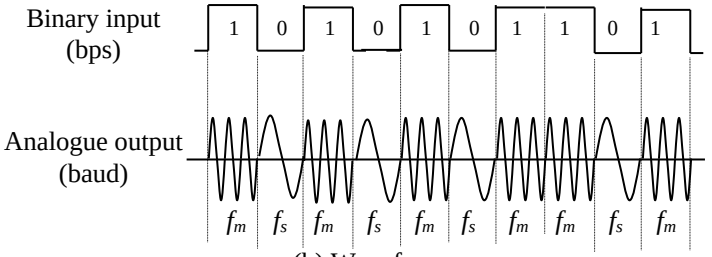
3.2.1 FSK Transmitter

FSK modulators are similar to conventional frequency modulators and are very often voltage-controlled oscillator (VCO) as shown in Fig.3.2. The output of binary FSK modulator is a step function in the frequency domain. As the binary input changes

from a logic 0 to a logic 1, and vice versa, the FSK output shifts between two frequencies: a space or logic 0 frequency and a mark or logic 1 frequency. Thus, the output rate of change is equal to the input rate of change.



(a) FSK Transmitter



(b) Waveforms

Fig.3.2 Binary FSK Modulator

Bit Rate and Baud Rate

In digital modulation, the bit rate, in bits per second, is the rate of change at the input to the modulator. Alternatively, the baud rate is the rate of change at the output of the modulator and is equal to the reciprocal of the time of one output signaling element. Henceforth, baud is the line speed in symbols per second.

3.2.2 Bandwidth and Modulation Index of FSK

The fastest rate of change occurs when the binary input is a series of alternating 1's and 0's: namely, a periodic square wave

as indicated in Fig.3.3. Consequently, if only the fundamental frequency of the input is considered, the highest modulating frequency is equal to one-half of the input bit rate. So, if the bit pulse width is T_b, the bit rate will be f_b and the highest modulating frequency is equal to $f_b/2$.

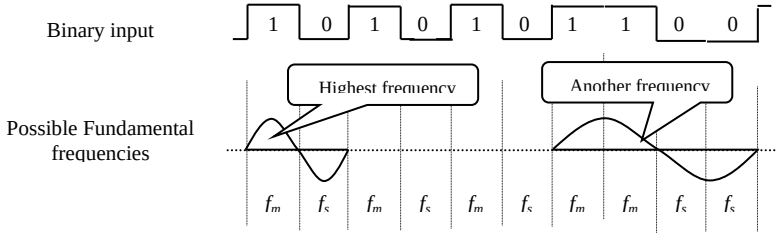

Binary input
1 0 1 0 1 0 1 1 0 0
Highest frequency
Another frequency
Possible Fundamental frequencies
fm fs fm fs fm fs fm fm fs fs

Fig.3.3: Highest Fundamental Frequency of Data Input

The rest frequency of the *VCO* is chosen such that it falls halfway between the mark and space frequencies. A logic 1 at the input shifts the VCO from its rest frequency to the mark frequency, and a logic 0 shifts its frequency to the space frequency. Since binary FSK is a form of frequency modulation, the formula for modulation index used in FM is also valid for binary FSK as:

$$MI = \frac{frequency\ deviation}{\text{mod}ulating\ frequency} = \frac{\Delta f}{f_{data}} \qquad (3.4)$$

The worst-case or widest bandwidth occurs when both the frequency deviation Δf and the modulating frequency f_{data} are at their maximum values. The peak frequency deviation Δf is half the difference between mark f_m and space f_s frequencies. It depends on the amplitude of the modulating signal. The modulating frequency f_{data} is equal to the fundamental frequency of the binary input, which under worst-case condition is equal to one half of bit rate f_b:

$$MI = \frac{|(f_m - f_s)/2|}{f_b/2} = \frac{|f_m - f_s|}{f_b} \qquad (3.5)$$

In binary FSK the modulation index *MI* is generally kept below 1.0 to produce a narrow band FM output spectrum. The

bandwidth is then determined from the Bessel functions table. For a modulation index between 0.5 and 1.0, either two or three sets of significant side frequencies are generated. Thus, the minimum bandwidth of binary FSK is two or three times the input bit rate.

3.2.3 FSK Receiver

At the reception, there are two ways to detect FSK signal and returns binary data signal.

Noncoherent Detection, where we do not have the presence and knowledge of the carrier frequency in the future. As shown in Fig.3.4.a, the signal coming from the transmitter is divided into two parts. When the frequency f_1 is the signal, it passes through the upper filter (BPF) only, and then be disclosed through the envelope detector to the operational amplifier (Op-Amp). When the frequency is f_0 its referred scroll through the bottom filter (BPF) only, and then it is disclosed through the envelope detector to Op-Amp. Finally, is to generate the original impulses through bilateral retrieval circuit (Binary Restoration).

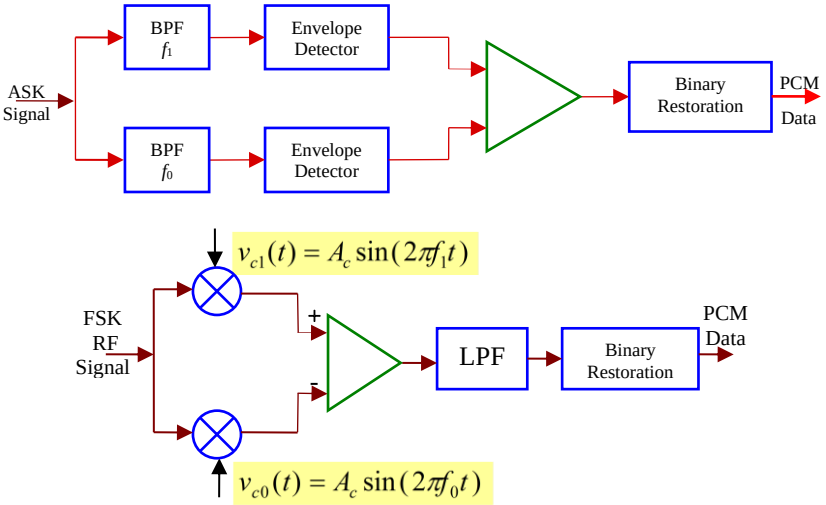


Fig.3.4: Noncoherent and Coherent Detection of FSK

Coherent detection, where we need a complete knowledge of the exact carrier frequency on reception. As in Fig.4.b, the received signal is applied into two multipliers, at f_1 and f_0, then to the difference Op-amp to the low-pass filter, and finally original impulses are generating through binary restoration circuit.

Binary FSK has a poorer error performance than PSK or QAM. Its use is restricted to low-performance, low-cost, asynchronous data modems that are used for data communication over analogue, voice band telephone lines.

3.2.4 Bandwidth of FSK

The approximate bandwidth for FSK signal is given by Carson's rule as follows in terms of the frequency deviation Δf and the bandwidth of the digital modulation waveform B:

$$B_{FSK} = 2(\Delta F + B) \tag{3.6}$$

For alternating 1 and 0, the bandwidth equals the bit rate $B=R$:

$$B_{FSK} = 2(\Delta F + R) \tag{3.7}$$

3.2.5 Bell 103-type FSK Modem

Keyboard-type computer terminals are often used for communication with a remote computer via dial-up telephone lines. ***Dial-up*** means that the computer terminal user calls the computer facility on a telephone and uses the telephone connection for data communication. The modem (modulator and demodulator) is connected to the phone line at each end as shown in Fig.3.5.

Two FSK frequency bands are used (one around 1 kHz and another around 2 kHz) so that it is possible to talk and listen simultaneously (***full-duplex***). The standard mark and space frequencies are shown in Table 3.1 where the peak to peak deviation is $2\Delta f$ =200 Hz.

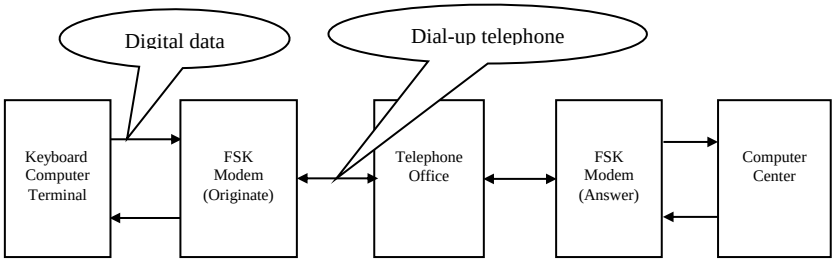


Fig.3.5: Computer Communication Using FSK Signaling

Table 3.1 Mark and Space Frequencies for the Bell Type 103 Modem

Mode	Data	Originate Modem	Answer Modem
Transmit frequencies	Mark (binary 1)	f_1 = 1270 Hz	f_1 = 2225 Hz
	Space (binary 0)	f_2 = 1070 Hz	f_2 = 2025 Hz
Receive frequencies	Mark (binary 1)	f_1 = 2225 Hz	f_1 = 1270 Hz
	Space (binary 0)	f_2 = 2025 Hz	f_2 = 1070 Hz

3.2.5 Minimum Shift Keying MSK

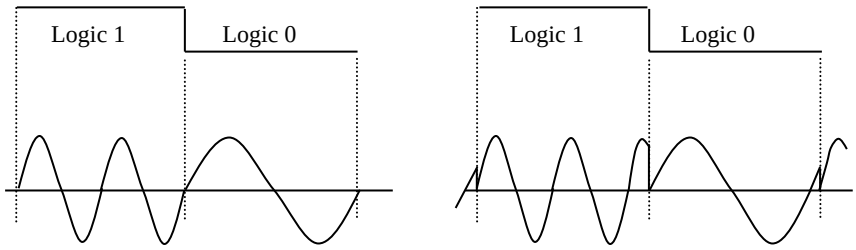
Minimum shift keying (MSK) is a form of continuous phase frequency shift keying (CPFSK). Essentially, MSK is binary FSK except that the mark and space frequencies are synchronized with the input binary bit rate.

Synchronous means that there is a precise time relationship between them. The mark and space frequencies are selected such that they are separated from the center frequency by an exact odd multiple of one-half of the bit rate f_b.

$$f_m \,\&\, f_s = n\frac{f_b}{2} \qquad (3.8)$$

This ensures that there is a smooth phase transition in the analog output signal when it changes from mark to a space frequency, or vice versa.

Fig.3.6 shows a comparison between MSK and FSK analog output signal whereas the phase discontinuity criterion is shown.



(a) Continuous Phase MSK (b) Non-continuous FSK

Fig.3.6: Comparison of the Phase Continuity between MSK and FSK

When phase discontinuity occurs, as in conventional binary FSK, the demodulator has trouble following the frequency shift, consequently an error may occur.

Therefore, MSK has a better bit error performance than conventional FSK for a given signal to noise ratio. Also it saves bandwidth as illustrated above.

However, the main drawback of MSK is that it requires synchronizing circuits and therefore is more expensive to implement.

3.3 Amplitude Shift Keying or On-off Keying

In amplitude shift keying, ASK, the amplitude of the carrier switches between two amplitudes. Or simply it could be switched between; zero (off state) and some predetermined amplitude (on state). In such a case it has been termed as on-off-keyed OOK. Assume a sequence of binary pulses as shown in Fig.3.7. The 1's turn on the carrier of amplitude *A* whereas the 0's turn it off.

It is clear that the spectrum of the OOK signal will depend on the particular binary sequence to be transmitted. However, the amplitude modulated OOK signal is the double sideband suppressed carrier given by:

$$f_{OOK}(t) = f_{ASK}(t) = A\, f(t) \cos \omega_c t \qquad (3.9)$$

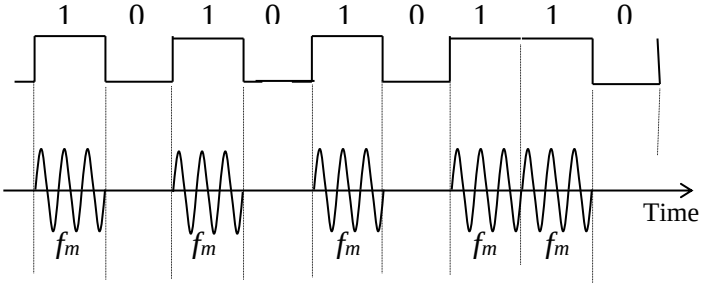


Fig.3.7: OOK Signal

Where *f(t)* equals 1 or 0. Generally, the spectrum of OOK signal is given as:

$$F_{OOK}(\omega) = F_{ASK}(\omega) = \frac{A}{2}\left[F(\omega-\omega_c) + F(\omega+\omega_c)\right] \qquad (3.10)$$

Assume the digital signal *f(t)* to be a single rectangular pulse (that is the special case of a binary data in which all symbols are 0 except for one 1). For a pulse of amplitude *A* and duration *T*, the spectrum of OOK modulator is given by:

$$F_{OOK}(\omega) = \frac{AT}{2}\left[Sa\left\{\frac{(\omega-\omega_c)T}{2}\right\} + Sa\left\{\frac{(\omega+\omega_c)T}{2}\right\}\right] \qquad (3.11)$$

For the case of alternating 1's and 0's, the spectrum is just the (sin x) /x. That is the spectrum of a pulse of width *T* and period 2*T* which is translated to frequency f_c as in Fig.3.8.

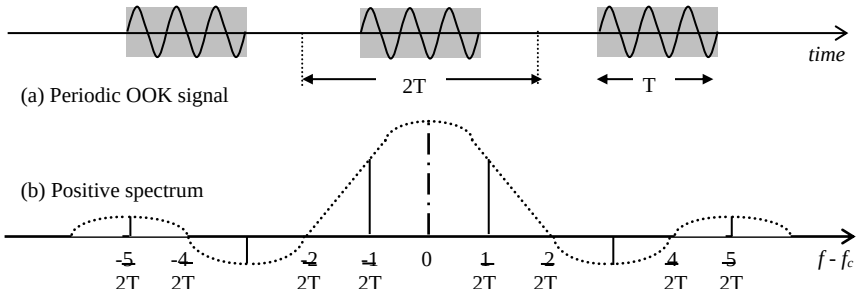


Fig.3.8: Spectrum of Periodic OOK Signal

3.4 Phase Shift Keying PSK

Phase shift keying, PSK, is similar to conventional phase modulation, PM, except that the input signal is a binary digital signal and a limited number of output phases are possible. With binary phase shift keying, BPSK, two output phases are possible for a single carrier frequency. One output phase represents a logic 1 and the other represents a logic 0. With a carrier amplitude V_c, and frequency ω_c, PSK voltage waveform for binary digital modulating signal *f(t)* is given by:

$$v(t) = V_c f(t) \sin \omega_c t = \begin{cases} +V_c \sin \omega_c t, & f(t) = +1 \\ -V_c \sin \omega_c t, & f(t) = -1 \end{cases} \qquad (3.12)$$

So, the carrier amplitude remains constant, whereas its phase shifts by 180^o. Recall, carrier phase shift rate equals the input rate.

3.4.1 BPSK Transmitter

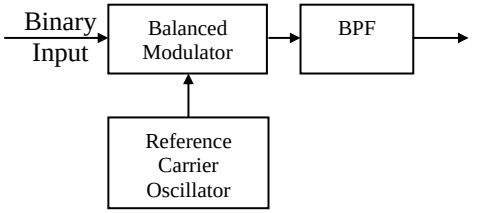


Fig.3.10: BPSK Modulator

A simplified block diagram of BPSK is shown in Fig.2.10 where the balanced modulator acts as a phase reversing switch. The carrier is transferred to the output either in phase or 180^o out of phase with respect to the reference carrier oscillator. The circuit of a balanced ring modulator is shown in Fig.3.11. The digital voltage must be much greater than the peak carrier voltage for proper operation.

- For logic 1: D1 and D2 are ON while D3 and D4 are OFF, carrier voltage across T2 is in phase with the carrier voltage across T1 or the reference oscillator.
- For logic 0: D1 and D2 are OFF while D3 and D4 are ON, carrier voltage across T2 is 180^o out of phase with the reference oscillator.

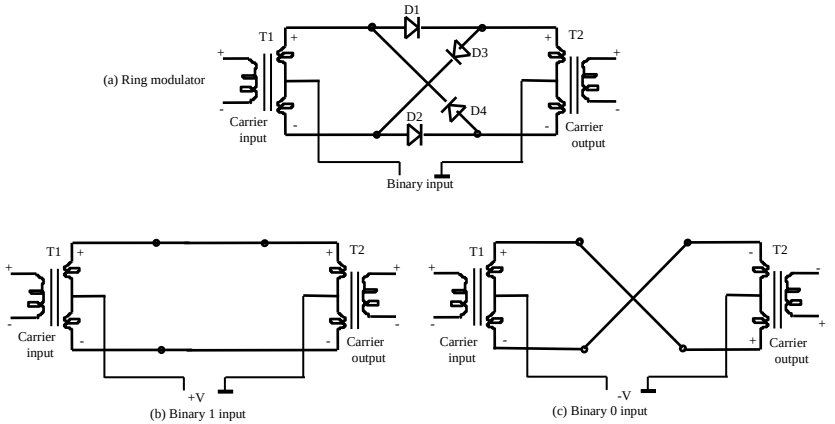
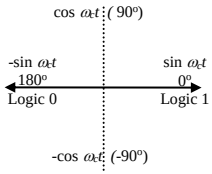


Fig.3.11: Balanced Ring Modulator

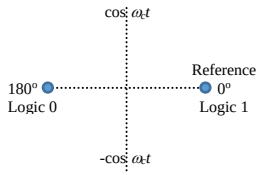
Fig.3.12 shows the truth table, phasor and constellation diagrams for a BPSK. The constellation diagram is similar to the phasor diagram except that the entire phasor is not drawn; only the relative positions of the peaks of the phasors are shown.

Binary Input	Output Phase
Logic 0	180°
Logic 1	0°

(a) Truth table



(b) Phasor diagram



(c) Constellation diagram

Fig.3.12: BPSK Representation

3.4.2 Bandwidth of BPSK

A balanced modulator is a product modulator where the carrier is multiplied by the binary data (either +1 or –1). Each time the input logic condition changes, the output phase changes. So, for BPSK, the baud rate (output rate of change) is equal to the input rate. Also, the widest bandwidth occurs when the input binary data is an alternating 1/0 sequence. As a product modulator, the output of the BPSK modulator is given by:

$$output = \sin \omega_a t \sin \omega_c t = \frac{1}{2}\cos(\omega_c - \omega_a)t + \frac{1}{2}\cos(\omega_c + \omega_a)t$$

Consequently, minimum double-sided Nyquist bandwidth is given:

$$B_{BPSK} = (\omega_c + \omega_a) - (\omega_c - \omega_a) = 2\omega_a = 2(f_b / 2) = f_b$$

So, the minimum bandwidth required to pass the worst-case BPSK output signal is equal to the input bit rate. The output phase of BPSK modulator is shown in Fig.3.13.

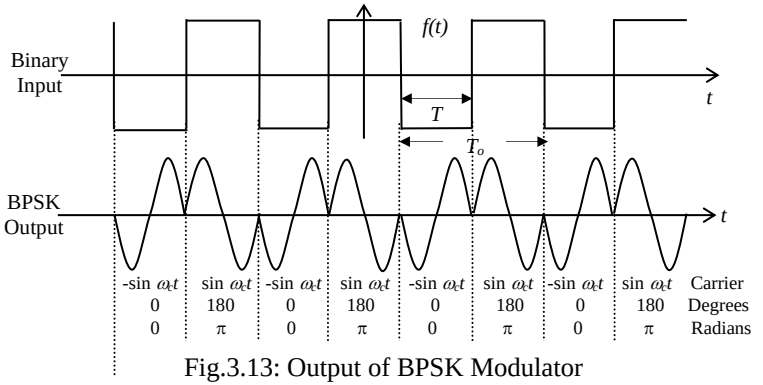


Fig.3.13: Output of BPSK Modulator

3.4.3 BPSK Receiver

Fig.3.14 shows the block diagram of BPSK receiver. The coherent carrier recovery circuit detects and regenerates a carrier signal that is both frequency and phase coherent with the original transmit carrier. The output of the balanced modulator is the product of the two inputs (BPSK signal and the recovered carrier). The LPF separates the recovered binary data from the complex demodulated spectrum. The demodulation process is as follows:

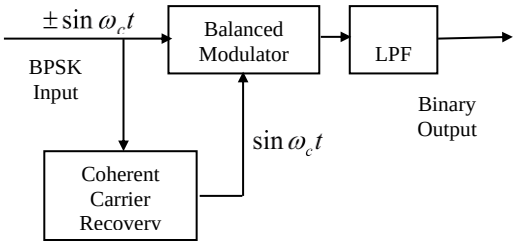


Fig.3.14: BPSK Receiver

- For a BPSK input $+sin\ \omega_c t$ (logic 1), the output of the balanced modulator is:

$$Output = \sin\omega_c t \sin\omega_c t = \sin^2\omega_c t = \frac{1}{2}(1-\cos 2\omega_c t) = \frac{1}{2} - \frac{1}{2}\cos 2\omega_c t$$

$$Filter\ output = +\frac{1}{2} \quad dc\ voltage \equiv Logic\ 1$$

- For a BPSK input $-sin\ \omega_c t$ (logic 0), the output of the balanced modulator is:

$$Output = -\sin\omega_c t \sin\omega_c t = -\sin^2\omega_c t = -\frac{1}{2}(1-\cos 2\omega_c t)$$

$$Filter\ output = -\frac{1}{2} \quad dc\ voltage \equiv Logic\ 0$$

3.5 *M*-ary Encoding Systems

With the binary digital communications systems we have considered so far, one of only two possible signals can be transmitted during each signaling interval. In an *M*-ary system, one of *M* possible signals may be transmitted during each signaling interval, where $M > 2$. Thus binary data transmission is a special case of *M*-ary transmission. With digital modulation, very often it is advantageous to encode at a level higher than binary, e.g., 4PSK and 8PSK. Each possible transmitted signal of an *M*-ary message sequence is referred to as "symbol". Mathematically, the number of bits per symbol "*n"* is related to the number of possible signals "*M"* by the following:

$$n = \log_2 M \quad or \quad M = 2^n \tag{3.13}$$

3.5.1 Quaternary or Quadrature Phase Shift Keying, QPFK

Quaternary phase shift keying, QPSK, is another form of angle modulated, constant envelope digital modulation, and four possible signals ($M = 4$). Four output phases are possible for a single carrier frequency.

The binary input data are combined into groups of 2 bits called dibits. Each dibit code generates one of the four possible output phases. For each 2- bit clocked into the modulator, a single output change occurs. So, the output baud rate is one-half of the input bit rate.

QPSK Transmitter

Basically, a QPSK modulator is a two BPSK modulators combined in parallel as illustrated in Fig.3.15 where:

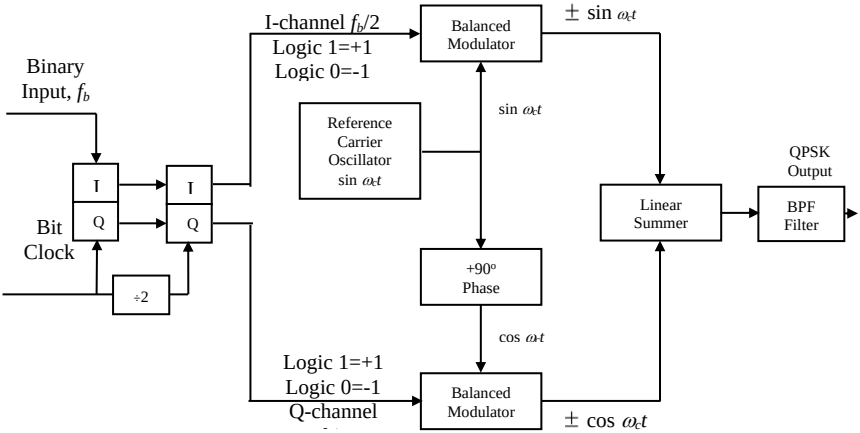


Fig.3.15: QPSK Modulator

- Two bits are clocked into the bit splitter.
- After both bits have been serially inputted, they are simultaneously parallel outputted.
- One bit is directed to I-channel to modulate the carrier that is in phase with the reference.
- The other bit is directed to Q-channel to modulate the carrier that is 90^o out of phase or in quadrature with the reference.
- When the linear summer combines the two quadrature signals (90^o out of phase), there are four possible phases as follows:

$$\pm \sin \omega_c t \pm \cos \omega_c t$$

Exercise 3.2:

Construct the truth table, phasor diagram, and constellation diagram of QPSK.

QPSK Bandwidth

Since the input data rate f_b is divided into two channels, the bit rate in either I or Q channel is equal to one-half of the input rate, i.e., f_b /2. Consequently, the highest fundamental frequency at the input of the balanced modulators is one-fourth of the input rate, i.e., f_b /4 as indicated in Fig.3.16.

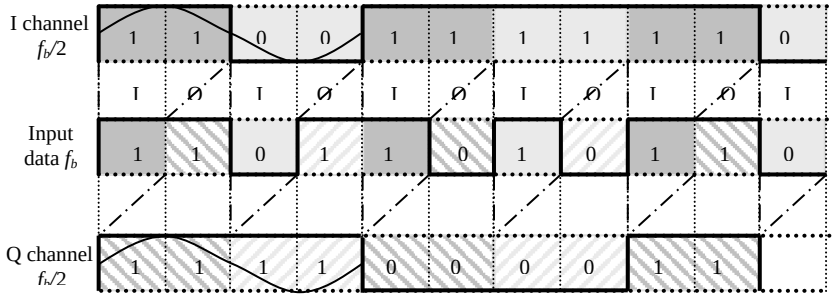


Fig.3.16: Highest Fundamental Frequency

The output of the balanced modulators requires a minimum double-sided Nyquist bandwidth that is twice the highest fundamental frequency at their inputs, i.e., twice f_b /4= f_b/2. Hence, the minimum bandwidth of QPSK is less than the incoming bit rate so that the bandwidth is compressed to f_b/2 only.

The output of the balanced modulator can be expressed as the product of I or Q channel sin $\omega_a t$ by the carrier sin $\omega_c t$:

$$Balanced = \sin \omega_a t \sin \omega_c t = \sin 2\pi \frac{f_b}{4} t \sin 2\pi f_c t$$

$$Balanced = \frac{1}{2}\cos 2\pi (f_c - \frac{f_b}{4})t - \frac{1}{2}\cos 2\pi (f_c + \frac{f_b}{4})t$$

So, the output frequency spectrum extends from f_c-f_b/4 up to f_c+f_b/4 and the minimum bandwidth:

$$B_{QPSK} = f_c + \frac{f_b}{4} - \left(f_c - \frac{f_b}{4} \right) = \frac{f_b}{2} \qquad (3.14)$$

QPSK Receiver

The block diagram of QPSK receiver is shown in Fig.3.17 and operation is as follows:

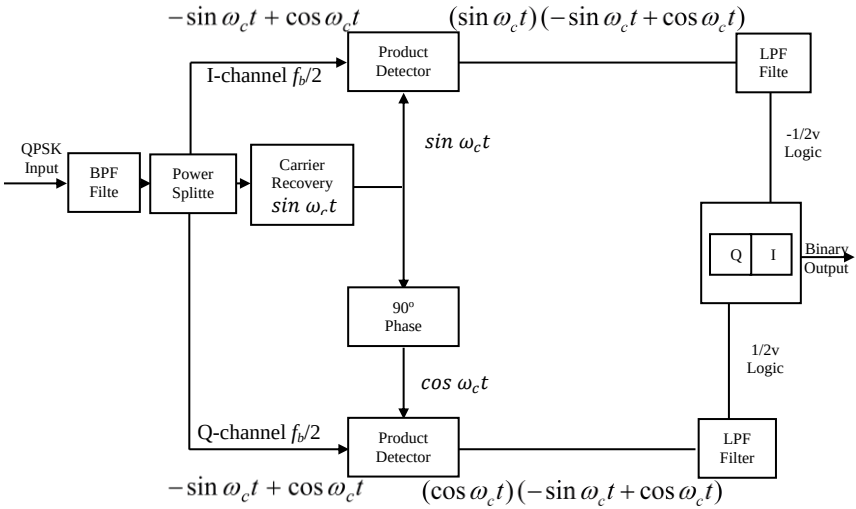


Fig.3.17: QPSK Receiver

- The power splitter directs QPSK signal into I and Q channels and carrier recovery circuit.
- The carrier recovery circuit reproduces the original transmit reference carrier.
- QPSK signal is demodulated in I and Q channels through the product detectors.
- The detectors outputs are fed to the bit combining circuit, where they are converted from parallel I and Q channels to a single binary output stream.

Offset Quadrature Phase Shift Keying OQPSK

OQPSK or Offset keyed QPSK (OKQPSK) is a modified form of QPSK where the bit waveforms on I and Q channels are offset or shifted in phase by one-half of a bit time. It can be implemented by adding a delay circuit as in Fig.3.18. Fig.3.19 shows the bit sequence alignment and the constellation diagram.

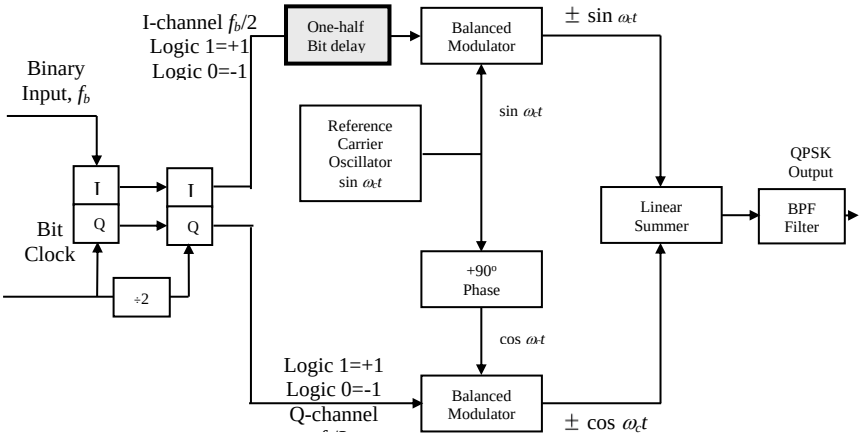
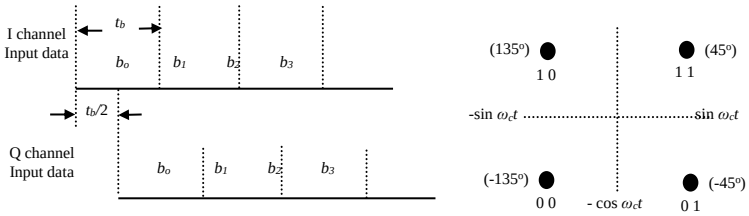


Fig.3.18: Offset QPSK Modulator



(a) Bit sequence alignment (b) Constellation diagram

Fig.3.19: OQPSK

In QPSK, a change in the input from 00 to 11 or 01 to 10 causes 180° shift in output phase. Since changes in I channel of OQPSK occur at the midpoints of Q channel bits, there is never more than a single bit change in the dibit code, and therefore there is never more than 90° shift in output phase which improves its performance.

A disadvantage of OQPSK is that changes in output phase occur at twice the data rate so that its minimum bandwidth is twice that of QPSK.

3.5.2 Eight-Phase PSK (8-PSK)

Eight phases PSK is an *M*-ary encoding technique where *M* equals 8; there are eight possible output phases. The incoming data bits are considered in groups of 3 bits, called tribits (that is $2^3 = 8$).

Truth table, phasor and constellation diagrams of 8PSK are indicated in Table 3.2, Fig.3.20, and Fig.3.21 respectively.

Table 3.2: 8-PSK

Binary input			8-PSK Output
A	B	C	Phase
0	0	0	-112.5
0	0	1	-157.5
0	1	0	-067.5
0	1	1	-022.5
1	0	0	112.5
1	0	1	157.5
1	1	0	067.5
1	1	1	022.5

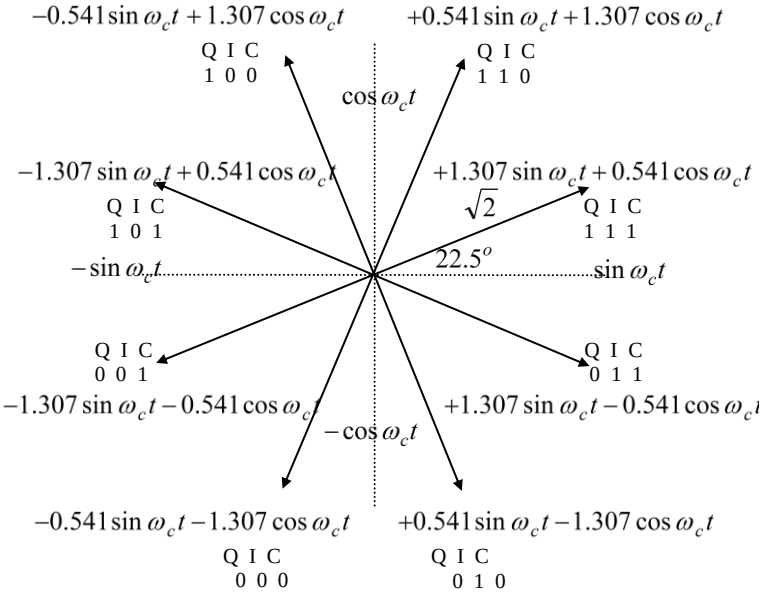


Fig.3.20: Phasor diagram of 8-PSK

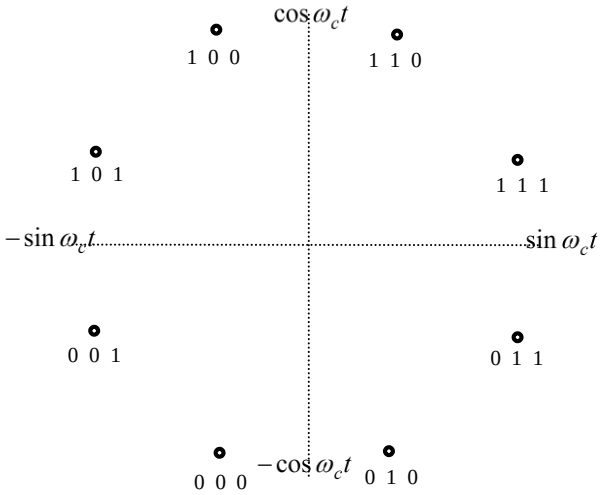


Fig.3.21 Constellation Diagram of 8-PSK

The transmitter of 8-PSK

Block diagram of 8-PSK modulator is shown in Fig.3.22.

- The incoming serial bit stream enters the bit splitter.

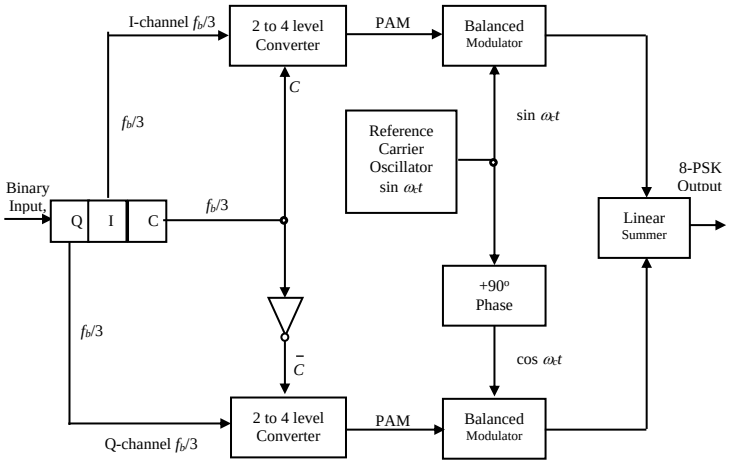


Fig.3.22: 8-PSK Modulator

- The splitter converted it into three parallel channels; in-phase channel (I), quadrature channel (Q), and control channel (C). The bit rate in each channel is then $f_b/3$.
- The bits in I and C channels enter the 2-to-4 level converter of I channel.
- The bits in the Q and $\bar{C}$ channels enter the 2-to-4 level converter of Q channel.
- These 4 levels when multiplied by the balanced modulator pair produce the 8-phase PSK.

2-to-4 Converter

The algorithm of the 2-to-4 level converter is quite simple. With the 2 parallel input bits 4 output voltages are possible because the 2-to-4 level converter is a digital-to-analog converter (DAC). I or Q bit determines the polarity of the output analog signal while C or $\bar{C}$ bit determines its magnitude (e.g., logic 1=1.307 v and logic 0=0.541 v). Thus, with the two magnitudes and the two polarities, four different output conditions are possible. This is an M level pulse amplitude modulated signal (PAM) where M=4.

According to Fig.3.22 the performance of the 2-to-4 level converter is illustrated in Fig.3.23 indicating its truth table and the possible voltage levels.

(a) I Channel Truth

I	C	Output
0	0	-0.541v
0	1	-1.307v
1	0	+0.541v
1	1	+1.307v

(b) Q Channel Truth

Q	$\bar{C}$	Output
0	1	-1.307v
0	0	-0.541v
1	1	+1.307v
1	0	+0.541v

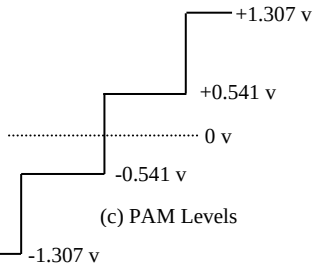


Fig.3.23: Operation of 2 to 4 Levels Converter

It should be noticed from constellation diagram of Fig.3.21 that the tri bit code between any two adjacent phase's changes by only one bit. This code is called the Gray code or, sometimes, the

maximum distance code. This code is used to reduce the number of transmission errors. If a signal were to undergo a phase shift during transmission, it would most likely be shifted to an adjacent phasor. Using the Gray code results in only a single bit being received in error.

The Bandwidth of 8-PSK

Since the data are divided into three channels, the bit rate in the I, Q, or C channel is equal to one-third of the binary data rate (i.e., $f_b/3$). Consequently, the highest fundamental frequency in I, Q, or C channel is equal to one-sixth of the input bit rate. Also the highest fundamental frequency in either PAM signal is equal to one-sixth of the input bit rate as indicated in Fig.3.24.

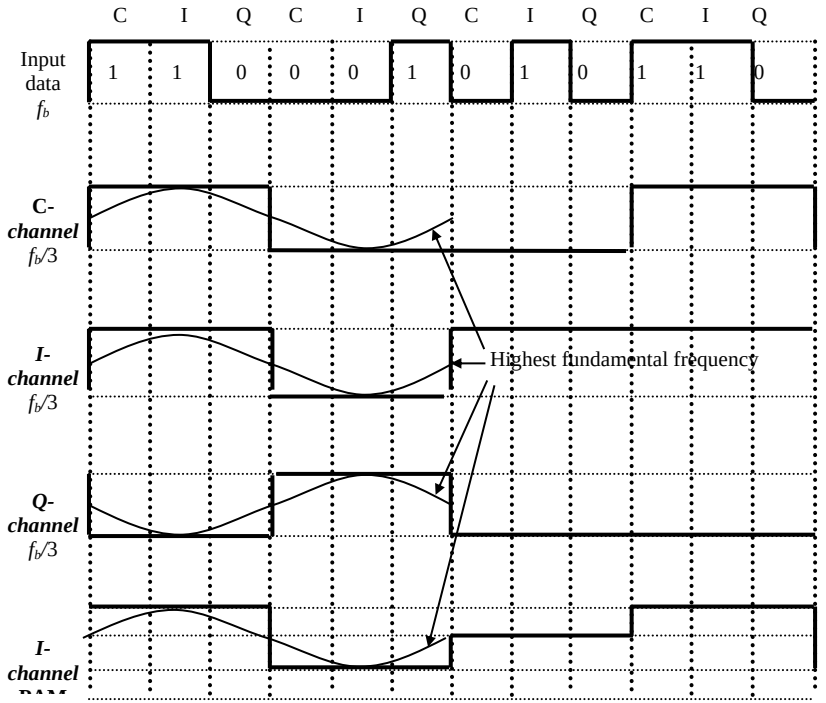

C I Q C I Q C I Q C I Q
Input data f_b
1 1 0 0 0 1 0 1 0 1 1 0
C-channel $f_b/3$
I-channel $f_b/3$
Highest fundamental frequency
Q-channel $f_b/3$
I-channel

Fig.3.24: Highest Fundamental Frequency of 8-PSK

The balanced modulators are product modulators so that their output is the product of carrier $\sin \omega_c t$ and PAM signal $X \sin \omega_a t$:

$$X(has\ 4\ levels) = \pm\cos 22.5 = \pm 1.307 \quad or \quad \pm\sin 22.5 = \pm 0.541$$

$$f_{Balanced} = X \sin \omega_a t \sin \omega_c t = X\left(\sin 2\pi \frac{f_b}{6} t\right)(\sin 2\pi f_c t)$$

$$= \frac{X}{2}\left[\cos 2\pi\left(f_c - \frac{f_b}{6}\right)t - \cos 2\pi\left(f_c + \frac{f_b}{6}\right)t\right]$$

Therefore, the bandwidth of 8-PSK can be estimated as follows:

$$B_{8-PSK} = \left(f_c + \frac{f_b}{6}\right) - \left(f_c - \frac{f_b}{6}\right) = \frac{f_b}{3} \qquad (3.15)$$

The Receiver of 8-PSK

Fig.3.25 shows block diagram of an 8-PSK receiver where:

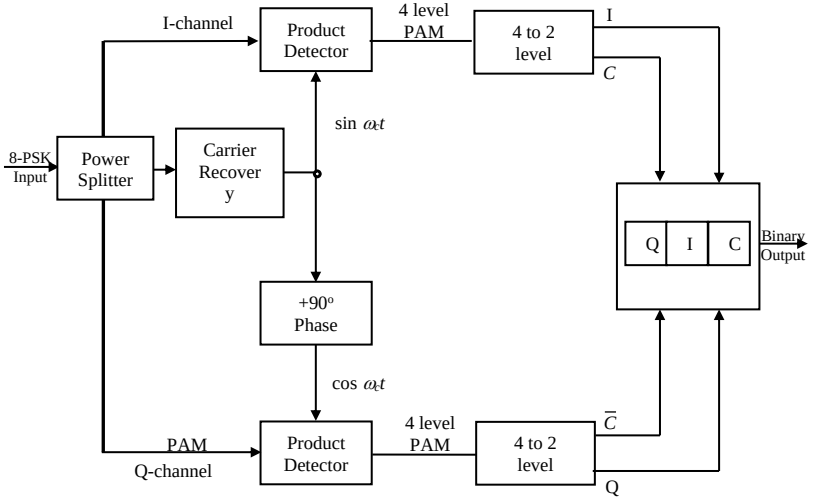


Fig.3.25: 8-PSK Receiver

- The power splitter directs the 8-PSK signal to the I and Q product detectors and the carrier recovery circuit.

- The carrier recovery circuit reproduces the original reference oscillator signal.
- The incoming 8-PSK signal is multiplied with the recovered carrier in I channel and the quadrature carrier (after 90^o phase shift) in Q channel.
- The outputs of product detectors (4 level PAM signal) are fed to the 4-to-2 level analog-to-digital converters.
- The outputs from I channel 4-to-2 level converter are I and *C* bits while those from Q channel are Q and *C* bits.
- The parallel-to-serial logic circuit coverts the I/*C* and Q/*C* bit pairs to serial I, Q, and C output data stream.

3.5.3 Sixteen-Phase PSK (16-PSK)

In 16-PSK there are 16 different output phases possible. The modulator acts on the incoming data in groups of 4 bits (2^4=16), called quad bits. So, the output phase does not change until 4 bits have been inputted into the modulator. Therefore, the output rate of change (baud rate) and the minimum bandwidth are equal to one-fourth of the incoming bit rate (i.e., $f_b/4$).

With 16-PSK, the angular separation between adjacent output phases is only 22.5^o. Therefore, the signal can undergo almost a $\pm 11.25^o$ phase shift during transmission and still retain its integrity. So, 16-PSK is highly susceptible to phase impairments introduced in the transmission medium and is therefore seldom used.

3.6 Quadrature Amplitude Modulation

Quadrature amplitude modulation (QAM) is a form of digital modulation where the information is contained in both the amplitude and the phase of the transmitted carrier. Eight QAM is an *M*-ary encoding technique where *M*=8. The output from 8-QAM modulator is not a constant-amplitude signal such as 8-PSK.

Transmitter of 8-QAM

8-QAM modulator is shown in Fig.3.26. The only difference between 8-QAM and 8-PSK transmitters is the omission of the inverter between the *C* channel and the Q product modulator.

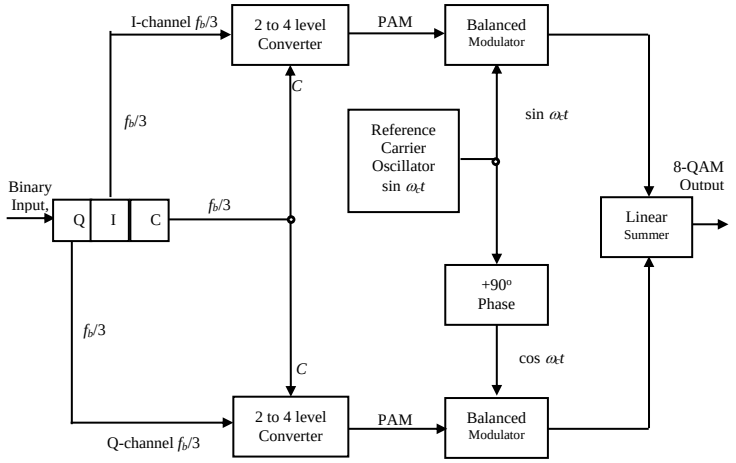


Fig.3.26: 8-QAM Modulator

- The incoming data are divided into I, Q, and *C* channels; each with a rate $f_b/3$.
- I and Q bits determine the polarity of PAM signal at the output of 2-to-4 level converters, and the *C* channel determines the magnitude.
- The magnitudes of PAM signals in I and Q channels are always equal in magnitude (because *C* bit is fed un-inverted to the converters of both I and Q channels) whereas their polarities depend on the logic conditions in I and Q bits.
- The truth table is illustrated in Table 3.3.

Exercise 2.3: For a tri bit input 000 (i.e., Q=0, I=1, and C=0):

i. Determine output amplitude and phase for 8-QAM.
ii. Repeat for possible inputs and record your answer in a table.
iii. Draw the phasor and constellation diagrams.

Table 3.3 Truth Table of 8-QAM

Binary Input			8-QAM Output	
Q	I	C	Amplitude	Phase
0	0	0	0.765 V	-135
0	0	1	1.848 V	-135
0	1	0	0.765 V	-45
0	1	1	1.848 V	-45
1	0	0	0.765 V	+135
1	0	1	1.848 V	+135
1	1	0	0.765 V	+45
1	1	1	1.848 V	+45

Bandwidth of 8-QAM

In 8-QAM, the bit rate in the I and Q channels is one-third of the input binary rate, the same as in 8-PSK. As a result, the highest fundamental modulating frequency and fastest output rate of change are the same as with 8-PSK. Therefore, the minimum bandwidth required for 8-QAM is $f_b/3$, the same as in 8PSK.

Receiver of 8-QAM

The receiver of 8-QAM is almost identical to the 8-PSK receiver shown in Fig.2.25. The differences are as follows:

- PAM voltage levels at the output of the product detectors.
- Binary signals at the output of the 4-to-2 level converters.

3.7 Bandwidth Efficiency of Digital Systems

The spectral efficiency, bandwidth efficiency or information density is often used to compare the performance of digital modulation techniques. It is the ratio of the transmission bit rate to the minimum bandwidth.

On other words, it indicates the number of bits that can be propagated through a medium for each hertz of bandwidth. The efficiency of various digital techniques that you have studied are illustrated in Table 3.4.

$$Efficiency = \frac{Bit\ Rate}{Bandwidth} = \frac{f_b}{B}\ \frac{b}{s}/Hz \qquad (3.16)$$

Table 3.4: Bandwidth Efficiency of Digital Modulation Techniques

Scheme	Encoding	Bandwidth, Hz	Baud rate	Efficiency, b/s/Hz
FSK	Single bit	$>f_b$	f_b	<1
BPSK	Single bit	f_b	f_b	1
QPSK	Di-bit	$f_b/2$	$f_b/2$	2
8-PSK	Tri-bit	$f_b/3$	$f_b/3$	3
8-QAM	Tri-bit	$f_b/3$	$f_b/3$	3
16-PSK	Quad-bit	$f_b/4$	$f_b/4$	4
16-QAM	Quad-bit	$f_b/4$	$f_b/4$	4

3.8 Carrier Recovery

3.8.1 Squaring Loop

A common method of carrier recovery for binary PSK is the squaring loop shown in Fig.3.27. Its operation is as follows:

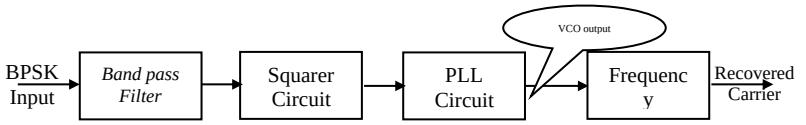


Fig.3.27: Squaring Loop Carrier Recovery for BPSK

- The received BPSK signal is filtered to reduce the spectral width of noise.
- Squaring circuit removes the modulation and generates the second harmonic of carrier.
- This harmonic is phase tracked by PLL.
- The frequency of PLL (VCO output) is then divided by 2 and used as a phase reference for the product modulators.

Since there is only two possible phases for BPSK, the mathematical operation will be as follows:

- If received signal is $+\sin\omega_c t$, output of the squaring circuit:

$$Output = (+\sin\omega_c t)^2 = \frac{1}{2}[1-\cos 2\omega_c t] \xrightarrow{filtered} -\frac{1}{2}\cos 2\omega_c t$$

- If received signal is $-\sin\omega_c t$, the output of squaring circuit:

$$Output = (-\sin\omega_c t)^2 = \frac{1}{2}[1-\cos 2\omega_c t] \xrightarrow{filtered} -\frac{1}{2}\cos 2\omega_c t$$

So, in both cases the output from the squaring circuit contained a dc voltage –0.5 v and a signal at twice the carrier frequency. The dc voltage is removed by filtering, leaving only $\cos 2\omega_c t$. Finally, the frequency divider return it to $\cos\omega_c t$.

Exercise 3.4:

Discuss the operation of the squaring loop when its input is $\sin(\omega_c t + \theta)$.

3.8.2 Costas Loop (Quadrature Loop)

The Costas loop shown in Fig.3.28 uses two parallel tracking loops (I and Q) to drive the product modulators that drive the product detector that drives the VCO.

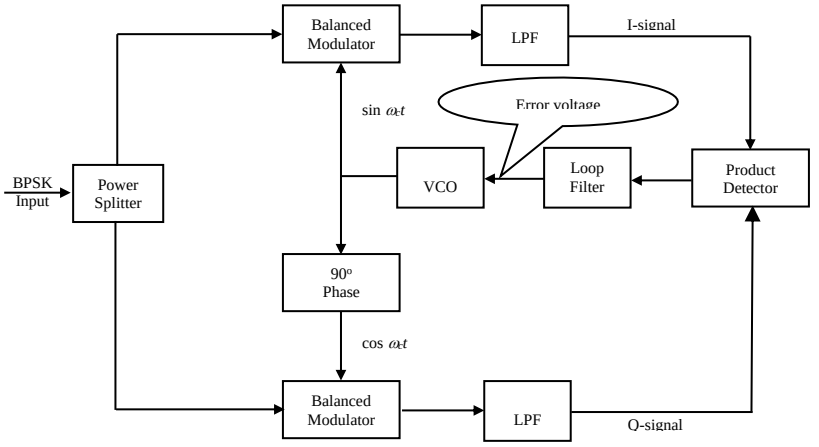


Fig.3.28: Costas Loop Carrier Recovery

Once the frequency of the VCO is equal to the suppressed carrier frequency, the product of the I and Q signals will produce an error voltage proportional to any phase error in the VCO. This error voltage controls the phase and thus the frequency of the VCO.

3.8.3 Remodulator

The remodulator shown in Fig.3.29 produces a loop error voltage that is proportional to twice the phase error between the incoming signal and the VCO signal. So, it has a faster acquisition time than either squaring or Costas loop.

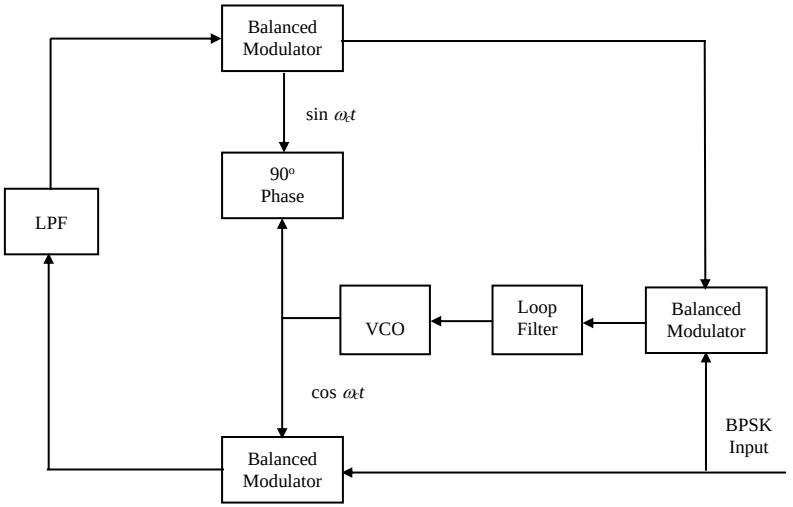
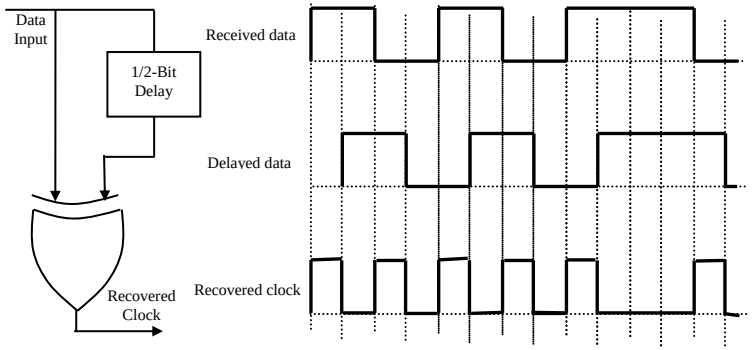


Fig.3.29: Remodulator Loop Carrier Recovery Circuit

2.9 Clock Recovery

Digital radio requires precise timing or clock synchronization between transmit and the receive circuitry. Fig.3.30 shows a simple circuit that is commonly used to recover clocking information from the received data. The recovered data are delayed by one-half a bit time and then compared with the original data in an XOR circuit. The frequency of the clock that is recovered with this method is

equal to the received data rate f_b. However, if the received data has extended period of successive 1's or 0's, the received clock would be lost.



(a) Circuit diagram (b) Timing diagram

Fig.3.30: Clock Recovery

2.10 Differential Phase Shift Keying

Differential phase shift keying (DPSK) is an alternative form of digital modulation where the input information is contained in the difference between two successive phases rather than the absolute phase. So, it is not necessary to recover a phase coherent carrier. Instead, a received data is delayed by one time slot and then compared to the next received bit.

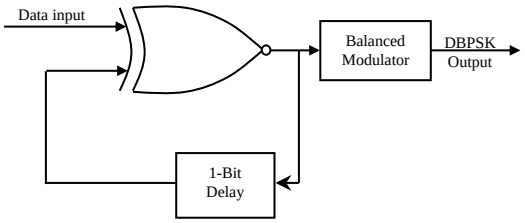


Fig.3.31 DBPSK Modulator

Fig.3.31 shows a simplified block diagram of a differential binary phase shift keying transmitter (DBPSK). An incoming information bit is XNORed with the preceding bit prior to the

modulator; if they are the same, the XNOR output is a logic 1; if they are different, it will be logic 0. An initial reference bit is assumed. The relationship between the input data, the XNOR output and the phase of the modulator output is shown in Fig.3.32.

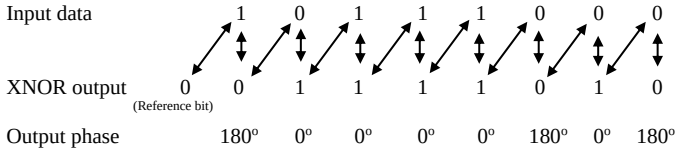


Fig.3.32: Timing Diagram of BDPSK Transmitter

As shown in Fig.3.33, the received signal is delayed by one bit time, then compared with the next bit in the balanced modulator. If they has the same phase, $+V$ is generated (logic 1), or otherwise $-V$ is generated (logic 0). The timing sequence is illustrated in Fig.2.34.

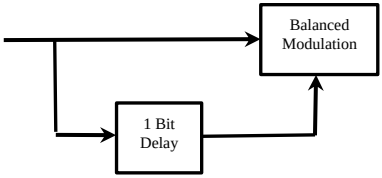


Fig.2.33 DBPSK Demodulator

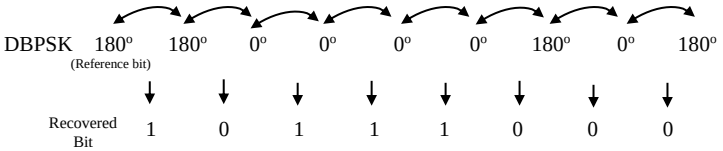


Fig.2.3:4 Timing Diagram of BDPSK Receiver

2.11 Probability of Error

Probability of error P_e is a theoretical expectation of the bit error rate BER for a given system whereas BER is an empirical (historical) record of the system's actual bit error performance. P_e is a function of the following:

- Carrier-to-noise ratio or average energy per bit-to-noise power density ratio.
- The number of possible encoding conditions.

The thermal noise N is expressed in terms of Boltzmann constant (K=1.38x10^{-23} J/K), the room temperature (T=290^{o}K), and the system bandwidth B Hz as follows:

$$N = KTB \quad (watts) = 10\log\frac{KTB}{0.001} \quad (dBm) \tag{3.17}$$

Where *dbm* means the power to mill watts. If the carrier power is C watts, then the carrier-to-noise power ratio is then:

$$\frac{C}{N} = \frac{C(watts)}{KTB(watts)} \tag{3.18}$$

$$\frac{C}{N}(dB) = 10\log\left(\frac{C}{KTB}\right) = C(dBm) - N(dBm) \tag{3.19}$$

Energy per bit-to-noise power density ratio E_b/N_o is the ratio of the energy of a single bit to the noise power present in 1 Hz of bandwidth. It is used to compare digital modulation systems that use different:

- Transmission rates (bps),
- Modulation techniques (e.g., PSK, FSK, MSK, OOK, …)
- Encoding techniques (e.g., QPSK, 8-PSK, 16-PSK, …).

Thus it normalizes all multiphase schemes to a common noise bandwidth allowing for a simpler and more accurate comparison of their error performance.

The average energy per bit E_b is related to the carrier power C and the bit duration T_b as:

$$E_b = CT_b = \frac{C}{f_b} \quad , \quad J/bit \tag{3.20}$$

$$E_b = 10\log\left(\frac{C}{f_b}\right) = 10\log C - 10\log f_b \quad , \quad dBJ \tag{3.21}$$

The noise power density N_o is the thermal noise power normalized to a 1 Hz bandwidth:

$$N_o = \frac{N}{B} \quad (watts / Hz) \tag{3.22}$$

So, the energy per bit-to-noise power density ratio E_b/N_o is given by:

$$\frac{E_b}{N_o} = \frac{C / f_b}{N / B} = \frac{CB}{N f_b} = \frac{C}{N} x \frac{B}{f_b} \tag{3.23}$$

$$\frac{E_b}{N_o}(dB) = 10\log E_b - 10\log N_o = 10\log\frac{C}{N} + 10\log\frac{B}{f_b} \tag{3.24}$$

2.12 Applications of Digital Modulation

FSK, PSK, or QAM has many applications in:

- Microwave radio and satellite systems with carrier frequencies from tens of megahertz to several gigahertz carrying voice, TV, data, etc.
- Voice band data modems with carrier frequencies between 300 and 3000 Hz.

Sheet 4

[1] Construct the truth table, phasor diagram, and constellation diagram of QPSK.

[2] Construct the truth table, the phasor diagram, and the constellation diagram of 8-PSK assuming the reference carrier amplitude as 1v.

[3] i- Follow up the signal flow in the modulator and the receiver of QPSK if its serial input data stream is 11100100.
ii- Draw the corresponding Q-PSK output signal.

[4] i- Follow up the signal flow in the modulator and the receiver of 8-PSK if its serial input data stream is 110101000.
ii- Draw the corresponding 8-PSK output signal.

[5] i- For a tri-bit input 0 0 0 (i.e., Q = 0, I = 1, and C = 0), determine the output amplitude and phase for 8-QAM modulator.
ii- Repeat for other possible inputs and record your answer in a truth table.
iii- Draw the phasor and constellation diagrams.

[6] Analyze the Costas loop carrier recovery circuit when the reference carrier is given by $sin\ \omega_c t$ whereas the input BPSK signal was $sin(\omega_c t + \theta)$.

[7] Analyze the remodulator carrier recovery circuit when the reference carrier is given by $sin(\omega_c t + \theta_1)$ whereas the input BPSK signal was $sin(\omega_c t + \theta_2)$.